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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appln No.:	10/044,777
Applicants:	Marc Chason et al.
Filed:	January 11, 2002
For:	SEMICONDUCTOR PACKAGE DEVICE AND METHOD
TC/A.U.:	2813
Examiner:	Jennifer M. Dolan
Docket No.:	CM001533I (72804)
Customer No.:	22242

Confirmation No. 8364

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REPLY BRIEF SUBMITTED UNDER 37 CFR §1.193(b)(1)

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The applicants respectfully submit this Reply Brief in response to the Examiner's Answer as mailed on June 15, 2004, in the above-captioned matter.

As a preliminary matter, an appendix of a copy of appealed claims 1 through 28 has been provided with the Reply Brief, as requested by the examiner.

Group 1

The applicants first note that the term "a complete underfilling" was used in the brief as a way to explain to the examiner that "Capote teaches disposing an underfill material on a die, and to then place that underfill material on another layer of underfill material as versus directly on a substrate." See *Applicants' Brief*, page 4. Thus, the applicants neither argue nor claim that "a complete underfilling" is a recited feature of claim 1. The examiner then, in an attempt to rebut this noted distinction of Capote, points to FIG. 18 of Capote (reproduced below for the convenience of the reader) as an example.

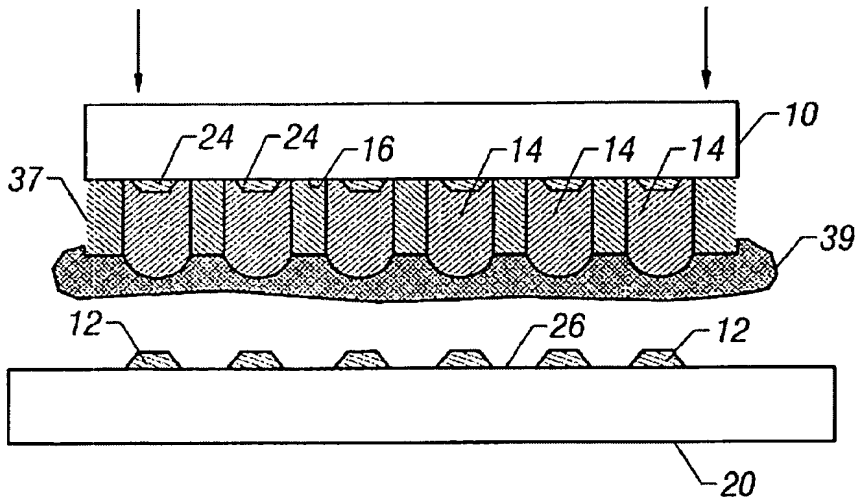

FIG. 18

However, FIG. 18 of Capote depicts exactly what the applicants are trying to show the examiner. Specifically, the semiconductor die (10), as shown in FIG. 18, is disposed with an underfill material (37) that is placed on top of another underfill material (39), instead of the substrate 20. No matter how much the examiner insists that the semiconductor die (10) with the underfill material (37) can simply be replaced with the interposer having a semiconductor die on one side, this combination does not disclose the claimed features, because Capote fails to disclose any "underfill material that is attached to the semiconductor die" as actually being placed on the substrate. Instead, the other underfill material, which is not attached to the die, is placed on the substrate. Thus, even if *arguendo* the semiconductor die of Capote is replaced with the interposer of Lin, the asserted combination does not disclose all the claimed features of "providing an interposer having at least one semiconductor die attached to a first side thereof" and "prior to placing the interposer on a printed wiring board, disposing a non-conductive underfill material on at least a portion of a second side thereof," as recited in claim 1.

As to the motivation to combine the cited references of Capote and Lin, the examiner insists that one skilled in the art would be motivated to combine Capote's teachings of a "pre-form underfill" with Lin's teachings of an interposer. However, the examiner also, at the same time, states that "Capote, in fact, makes no suggestion or teaching pertaining to a combination of underfill and interposer technologies." See *Examiner's Answer*, page 12. A complete reading of both references reveals that the references, in fact, distinctly teach away from such a combination.

In particular, the applicants respectfully disagree with the examiner's assertion that "Capote does not indicate that it would in any way be undesirable or inoperable to combine underfill and interposer technologies." See *Examiner's Answer*, page 12. Capote, in several places, notes the undesired result of the use of an interposer with an air gap: (1) "The air gap 103 between the chip and the substrate allows these two parts to expand and contract at relatively different rates thereby distorting the solder joints." See *Capote et al.*, Col. 1, lines 53-56; (2) "Unlike the previous interposer methods, there cannot be an air gap or separation between the underfill 104 and the chip 100 or the substrate 101." See *Capote et al.*, Col. 2, lines 18-20; and (3) "As a result, the underfilled flip chip assembly solder joint lifetime is greatly increased relative to that of an air gap flip chip solder joint." See *Capote et al.*, Col. 2, lines 18-20. From these descriptions of the air gap problems of the interposer and the fact that all the embodiments of Capote do not include an interposer or a die with an air gap, Capote, at the very least, discourages the reader from using an interposer or a die with an air gap.

Lin, on the other hand, teaches of the importance of including an air gap between the semiconductor die and the interposer for the easy removal and rework of the die. See *Lin*, Col. 5, lines 25-41. When viewing the Capote and Lin references in this context, they appear to both, in fact, teach away from each other, because inclusion of the air gap, or the lack of one, is an important feature for both references for opposite reasons. Specifically, Capote discourages the use of an interposer with an air gap because it distorts the solder joints of the chip and the substrate. Lin, in contrast, highlights the importance of the use of the interposer with an air gap for flexibility of removal of the die from the interposer. In fact, if one combined the Capote and Lin references as suggested by the examiner, the asserted combination actually defeats Lin's purpose of easy removal of the die from the interposer. For all these reasons, the applicants respectfully submit that the examiner has failed to establish any of the elements required for a *prima facie* case of obviousness. Specifically, in summary, the applicants respectfully submit that (1) there is no suggestion or motivation to make the combination as asserted because Capote and Lin teach away from one another, (2) there is no reasonable expectation of success because the asserted combination will defeat the purpose and benefits disclosed in Lin, and (3) even if *arguendo* the applicants accepted the examiner's arguments on obviousness, the asserted combination, nevertheless, does not disclose all the claimed features of claim 1 because Capote

does not disclose any underfill material that is attached to the semiconductor die being placed on the substrate.

Claims 14-20 are ultimately dependent upon Claim 1, which has been shown as allowable above. In addition, these claims introduce additional content that, particularly when considered in context with the claim or claims from which they depend, introduces additional incremental patentable subject matter.

Group 2

In regard to group 2, the applicants respectfully submit that the examiner oversimplifies the combination of Capote and Lin. Basically, the crux of the argument is that since Lin discloses solder balls (32) (e.g., interface electrodes) and Capote teaches a pre-formed underfill, it would be obvious to combine the two cited references. The examiner used FIG. 4 from Lin (reproduced below for the convenience of the reader) as the basis for the disclosure of the interface electrodes recited in claims 2-4 and 21-28. See *Examiner's Answer*, page 14.

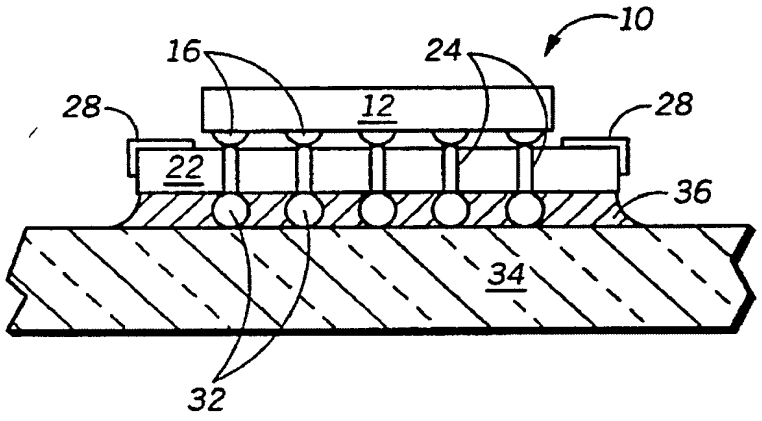

FIG. 4

The applicants reassert the arguments above relating to claim 1. Moreover, the applicants further emphasize that, even if the asserted combination was made, the assembly of device (10) disclosed in Lin would actually be more difficult, given the configuration of the chip. As a result, one skilled in the art would actually avoid making the asserted combination. Specifically, if the interposer with the interface electrodes is pre-filled with underfill material before being attached to the substrate as proposed by the examiner, this requires that the die (12), the solder bumps (16), the interposer (22), the vias (24), the solder balls (32), and the underfill 36 be correctly

aligned with one another before being placed on the substrate. However, with configuration of device (10) in Lin as shown in FIG. 4, it does not make sense to pre-assemble the semiconductor device 10, and not use the substrate as a stable surface for assembly. Thus, for all these reasons, the applicants respectfully submit that the Lin reference teaches away from the combination asserted by the examiner.

Group 3

The Examiner cites FIGS. 19-21 of Capote to anticipate the claimed features of claims 5-8. However, these figures of Capote relate to the method for creating the solder bumps of the first portion of the encapsulant (37), see *Capote*, Col. 10, lines 52-55, specifically the encapsulant that is not attached to the substrate 20. The applicants reassert the above arguments relating to claim 1. As a result, contrary to the Examiner's assertion, none of the cited references, alone or combined, discloses or suggests the interposer, as recited in claims 5-8, disposed with a non-conductive underfill material on at least a portion of a second side prior to being placed on a printed wiring board.

Group 4

In the Examiner's Answer, the examiner asserted that "curing at about 165 degrees would constitute 'low temperature drying,'" but the applicants did not find such a disclosure in the Capote reference. See *Examiner's Answer*, page 15. If an Official Notice based on any facts within the personal knowledge of the examiner is taken at this juncture, the applicants respectfully request that the examiner place an affidavit into the record under 37 CFR §1.104(c)(2) to detail these facts. As a result, the applicants can be afforded with the proper opportunity to contradict or explain, by affidavit or otherwise, such facts. See MPEP §2144.03.

Group 5

In regard to group 5, the examiner asserts that column 9, lines 59-62, of the Capote reference discloses the recited features of claims 12 and 13. However, the applicants note that this disclosure is made in reference to FIGS. 19-21, which have been noted earlier as relating to a method that pertains to the first portion of the encapsulant (37) that is not attached to the

substrate. The applicants, again, reassert the above arguments relating to claims 1 and 5-8, and respectfully submit that none of the cited references discloses the claimed features as recited in claims 12 and 13.

In summary, the applicants continue to respectfully submit that the distinct teachings of Capote and Lin, alone and particularly when taken in conjunction with the full teachings of each reference, neither permit an obvious combination that yields the claimed subject matter or even an unobvious combination of their various constituent elements to otherwise match the recitations of the claims. The applicants continue to argue that claims 1 through 28 are allowable in their present form.

This Reply Brief, along with an appendix of a copy of claims 1 through 28, is submitted in triplicate.

Respectfully submitted,

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APPENDIX

1. (Currently amended) A method comprising:

- providing an interposer having at least one semiconductor die attached to a first side thereof;

- prior to placing the interposer on a printed wiring board, disposing ~~an~~ a non-conductive underfill material on at least a portion of a second side thereof.

2. (Original) The method of claim 1 wherein providing an interposer includes providing an interposer having at least one interface electrode disposed on the second side thereof.

3. (Original) The method of claim 2 wherein providing an interposer having at least one interface electrode disposed on the second side thereof includes providing an interposer having at least one interface electrode comprising one of a solder bump and a solder ball disposed on the second side thereof.

4. (Original) The method of claim 1 and further comprising adding at least one interface electrode to the second side of the interposer.

5. (Currently amended) The method of claim 4 wherein adding at least one interface electrode to the second side of the interposer includes adding at least one interface electrode to the second side of the interposer after disposing the non-conductive underfill material.

6. (Currently amended) The method of claim 5 wherein disposing ~~an~~ a non-conductive underfill material includes disposing ~~an~~ a non-conductive underfill material on at least a portion of the second side thereof while simultaneously providing at least one aperture in the non-conductive underfill material.

7. (Currently amended) The method of claim 6 wherein adding at least one interface electrode to the second side of the interposer after disposing the non-conductive underfill material includes adding at least one interface electrode in the at least one aperture.

8. (Currently amended) The method of claim 5 and further comprising forming at least one aperture in the non-conductive underfill material and wherein adding at least one interface electrode includes adding at least one interface electrode in the at least one aperture.

9. (Currently amended) The method of claim 1 wherein disposing ~~an~~ a non-conductive underfill material includes disposing a plurality of material layers.

10. (Original) The method of claim 9 wherein disposing a plurality of material layers includes exposing at least one of the material layers to low-temperature processing.

11. (Currently amended) The method of claim 10 wherein exposing at least one of the material layers to low-temperature ~~drying~~ processing includes exposing each of the material layers to low-temperature drying.

12. (Currently amended) The method of claim 1 and further comprising removing at least a portion of the non-conductive underfill material to expose at least a portion of at least one interface electrode.

13. (Currently amended) The method of claim 12 wherein removing at least a portion of the non-conductive underfill material includes using at least one of chemical mechanical polishing, abrading, grinding, mechanical polishing, and laser ablation to expose at least a portion of at least one interface electrode.

14. (Original) The method of claim 1 wherein providing an interposer having at least one semiconductor die attached to one side thereof includes providing a plurality of interposers disposed substantially co-planar to one another, wherein at least some of the interposers each have at least one semiconductor die attached to one side thereof.

15. (Original) The method of claim 14 wherein providing a plurality of interposers includes providing a plurality of singulated interposers.

16. (Original) The method of claim 14 wherein providing a plurality of interposers includes providing a panel comprised of a plurality of interposers.

17. (Currently amended) The method of claim 14 wherein disposing ~~an~~ a non-conductive underfill material on at least a portion of the second side of the interposer includes

disposing ~~an~~ a non-conductive underfill material on at least a portion of the second side of at least some of the plurality of interposers.

18. (Currently amended) The method of claim 17 and further comprising, after disposing the non-conductive underfill material, singulating the interposers to provide singulated interposers.

19. (Original) The method of claim 18 and further comprising placing at least some of the singulated interposers into a carrier to facilitate subsequent placement of the singulated interposers on a printed wiring board.

20. (Original) The method of claim 19 wherein placing at least some of the singulated interposers into a carrier includes placing at least some of the singulated interposers into at least one of a tape and reel carrier, a waffle pack, and a matrix tray.

21. (Currently amended) A method comprising:

- providing a printed wiring board;
- providing at least one interposer having:
- a first side having at least one semiconductor die affixed thereto;
- a second side having:
- ~~an~~ a non-conductive underfilling material disposed thereon; and
- at least one interface electrode at least partially exposed through the non-conductive underfilling material; and
- disposing the at least one interposer on the printed wiring board.

22. (Original) The method of claim 21 wherein the at least one interface electrode comprises one of a solder ball and a solder bump.

23. (Currently amended) The method of claim 21 and further comprising further processing the at least one interposer on the printed wiring board to at least partially harden the non-conductive underfilling material.

24. (Currently amended) The method of claim 23 wherein further processing includes heating the non-conductive underfilling material.

25. (Currently amended) A device comprising:

a pre-placement interposer having:

- a first side having at least one semiconductor die affixed thereto; and
- a second side having:
- ~~an~~ a non-conductive underfilling material disposed thereon; and
- at least one interface electrode at least partially exposed through the non-conductive underfilling material.

26. (Original) The device of claim 25 wherein the interposer comprises means for physically and electrically coupling a semiconductor die to a printed wiring board.

27. (Currently amended) The device of claim 25 wherein the non-conductive underfilling material comprises adherence means for physically coupling the interposer to a printed wiring board.

28. (Currently amended)The device of claim 25 wherein the second side has a plurality of interface electrodes at least partially exposed through the non-conductive underfilling material.